IMPROVED DIFFERENTIAL LINEARITY PERFORMANCES OF HIGH SPEED WILKINSON-RECURSIVE SUBRANGING CONVERTERS

LUIGE VLĂDĂREANU

The paper presents a new method for Wilkinson Recursive Subranging (W-RS) conversion that ensures a high conversion rate and improved performance of differential and integral linearity. Starting from basic principles of W-RS conversion, which have been studied and presented by the author in other papers, we can reduce the conversion time from 2^{n+m} steps, corresponding to Wilkinson conversion, to $2^n + 2^m$ steps corresponding to the recursive conversion method which maintains performances of differential linearity specific to Wilkinson conversion. We have implemented a converter with a number of 32,000 conversion channels, for a medium conversion time of 2 MSPS with a 0.7% improved differential linearity by choosing for both steps an 8-bit conversion and taking into account the overlap of a bit for each step of the conversion used to perform digital connection. The new method presented in this paper is patented by the author.

1. INTRODUCTION

Improvement of performances of high speed and revolution converters has been approached in many aspects which have become concrete with new models of conversion developed during last years: recursive subranging conversion, multistep conversion, a new approach successive approximations conversion with switching capacitors networks, DELTA-SIGMA method, models which have generated an equal number of new architectures. These models have allowed obtaining of conversion speed and/or resolutions that were unthinkable only few years prior. Nevertheless, most of these models ensure minimal error of integral and differential non-linearity of $\pm 1/2$ LSB, insufficient in many applications. In such applications there is a need for linearity on a large domain of the transfer function of the converter at high speed and resolution. In the same time, very small non-linearity can determine severe harmonic distortions of the sampled signal.

The interest for these problems is well known at European level in the framework of EUROBALL project for development of new acquisition systems with applications in nuclear spectroscopy. The most well-known technique which ensures a high intrinsic uniformity of conversion channels is the Wilkinson method, which necessitates a longer conversion time, "sliding scale" method [9] applied to

Romanian Academy, Institute of Solid Mechanics, C-tin Mille 15, Bucharest 1, Romania

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successive approximation method based converters ensures a substantial improvement of channel width uniformity, but is insufficient for many applications. Several methods were suggested in order to improve performances of data acquisition system: coarse fuzzy coding, up-downward averaging and moving window deconvolution [8]. The present paper represents an original direction in reducing differential non-linearity and ensuring a high speed conversion model for data acquisition systems of physical experimental data.

2. RECURSIVE SUBRANGING ADC's

The recursive subranging ADC's represent a new generation of converters which ensure shorter conversion time and high resolution. They are a compromise between flash ADC, which ensures very short conversion time but has a large number of components and converters with successive approximations register SAR, which need a small number of components but achieve a comparison sequence on resolution bit. Thus, for a SAR converter with 2 μs the time needed for a comparison sequence is 24 μs on 12 bits, compared to much less than 1 μs that a flash converter needs, but having 4096 comparators. Recursive sub ranging ADC's reduce the number of steps for determining the conversion value by a recursive mean of using for each step. Respectively, the residual voltage between input voltage and the coarse conversion result is gained up at the conversion range and stored in a sample-and-hold (SHA) amplifier, becoming input voltage for the next step.

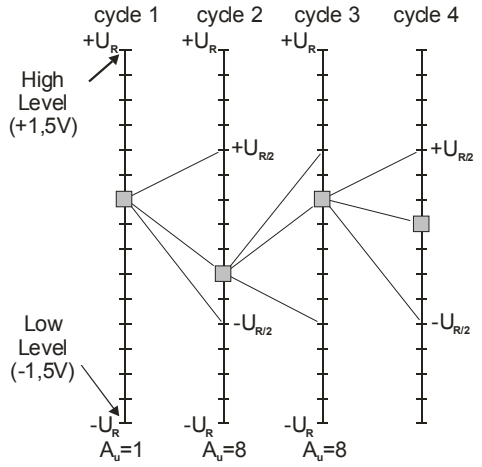

Fig. 1

The relationship of recursive for the determination of the conversion digital value is shown in Fig. 1, upon the basis of 4 cycles with coarse conversion on each cycle

and an 8-fold amplification for bringing back the residual tension into the conversion range.

3. W-RS CONVERTER ARCHITECTURE

The application of advanced linear and digital integrated circuits has allowed the ADC's to sum up the advantages of high speed and high integral and differential linearity. To achieve these features the new high speed Wilkinson-recursive sub ranging ADC's architecture divides the standard single conversion cycle of Wilkinson type in two steps. In the first step:

– the Wilkinson ADC is used as a coarse encoder of the input peak voltage and the first 7 bit digital output is latched in the dedicated part of the main counter (MSB part);

– a DAC with special features, high speed on 7 bit resolution achieving a THD better than 0.0003%, generates an analog signal corresponding to the 7 bit coarse conversion but with 1 LSB at 18 bits precision;

– a sum-amplifier provides the difference between input signal and DAC output, which is amplified by 32 to normalize it at 1/4 of the full-scale input signal.

In the second step:

– the same Wilkinson type ADC is used as a fine encoder of the above normalized residual signal, corresponding to the last 5 bits;

– the 5 bits digital output is latched in the other part of the main counter (LSB part).

The ADC is intended to be used in pulse spectrometry with random distribution, *i.e.* nuclear instrumentations and high speed data acquisitions with low DNL error and last time in the advanced ultrasonic measures.

Having a fast event as an input signal the graphic representation of the Wilkinson conversion is shown in Fig. 2, where STR C is a signal internally generated by the peak detector of the Wilkinson ADC at the start of the conversion, STOP C is a signal internally generated at end of the conversion.

Starting out from the basic principle of conversion models, presented and studied by this scientific group in many other papers [3–5], one can reduce the conversion time from 2^{n+m} steps needed for Wilkinson conversion down to 2^n+2^m steps corresponding to the new model based on the recursive method while maintaining high performances of differential linearity specific to the Wilkinson method. This means that for an ideal A/D converter with the clock frequency of 400 MHz the conversion time is reduced from 10μs to 0.4 μs for a two-step conversion of 7+5 b, with an increase of 25 times of the conversion speed respectively from 100KSPS up to 2.5 MSPS delivering high performances of the differential and integral linearity.

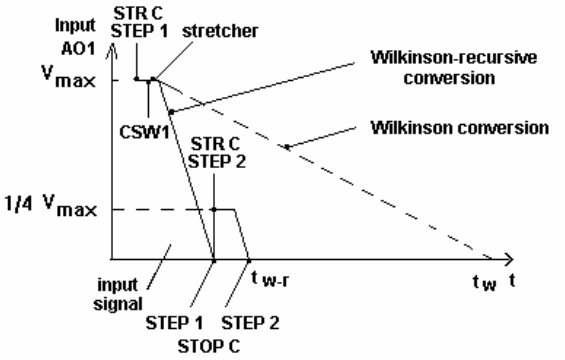

Fig. 2

The very good differential linearity of the Wilkinson converter is due to the fact that, in order to determine the digital code, all channels are scanned until the one corresponding to the input voltage is reached, while the successive approximation register converters determine the digital code by introducing weights, as powers of 2 that introduces profound discontinuities.

Integral linearity of the classical Wilkinson converter is much weaker in comparison with the RAS converter since integral linearity acts as the sum of small differential non-linearity with slow variation in the same direction and can be influenced by the impedance of the current generator, by the variation of long term parameters, etc. Due to digital correction in recursive conversion one can ensure a substantial improvement of integral linearity as well, by overlapping one bit from the two steps of conversion.

4. THE IMPLEMENTATION OF THE METHOD

The implementation of this method on 12-b, two step, recursive sub ranging ADC is shown in Fig. 3 with timing diagram in Fig. 4. The function is as follows: at start command, SHA1 is commanded to sampling; after another 200 ns, when the control error is lower than 1% at the SHA1 output, SHA2 is driven to sampling; after 300ns, when the control error is smaller than 0.01% SHA2 passes onto hold mode; the output is digitally converted on 7-b, encoded and digitally stored, the MSB being obtained; after an acquisition time of 500ns for SHA2, the settle error is less than 0.01% which allows passing to hold and storing for the last 6-b; by means of the digital correction of the 13-b, that is 7+6 bits with overlap, we obtain the converter resolution on 12-b. Conversion time is substantially reduced both by the overlap of the acquisition times and by reducing the number of steps in accomplishing the conversion. The 64 gain for ARz does not represent an impediment by choosing a high slew rate op-amp and short settle time.

The block diagram of the experimental model of new architecture for a high speed Wilkinson converter based on the Wilkinson-recursive sub ranging combination is shown in Fig. 5. The Wilkinson ADC allows a fast event detection and digital conversion; it replaces the flash ADC of Fig. 3, by determining the first 7 coarse bits, having on 12-b accuracy and the differential nonlinearity error less than 1% of LSB. The digital result of the first Wilkinson is analogically converted by a D/A converter of 7-b, but 18-b accuracy which allows a corresponding precision of the DNL error of the final conversion result.

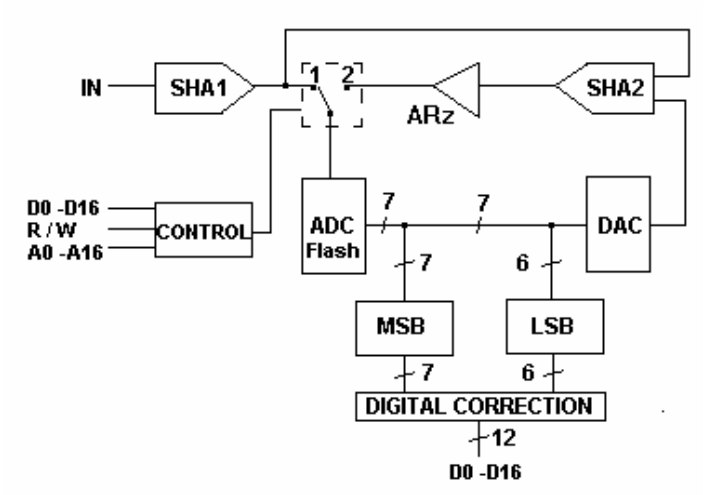

Fig. 3

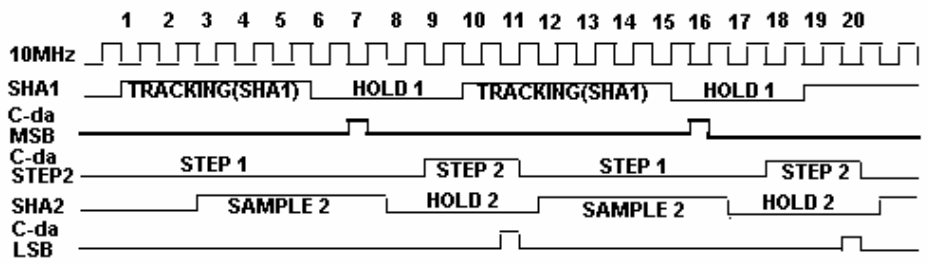

Fig. 4

By comparison with the holded input signal in C capacitor, we obtain the residual tension and the 32 inter-stage gain is brought back into the Wilkinson conversion range. In the second step, we determine the next 5 fine bits.

Because of the accuracy of the Wilkinson Converter and of the D/A converter, no digital correction of the error is needed. In case of high values of the offset, gain or integral nonlinearity (INL) errors, their self-calibration can be made. The 7-b and 5-b can be read in each step, or at the end of the conversion, in which case they will be stored in some latches. For the implementation of the circuit, a controller generates the control signals, according to the sequential diagram in Fig. 6. Their significance and delay times are given below:

– t_{w1} – the time necessary for stabilization of the AO1 output;

– t_{w2} – the stabilization time of the D/A C current, after having made the conversion in step one, and for the stabilization of the AO3 output.

– t_{w3} – delay necessary for a new start command of the Wilkinson ADC between step one and two;

– t_{w4} – dead time after which a new conversion can be started, necessary for the reset of the latches into the controller.

The SW2 switch is necessary for not bringing the AO3 output in saturation or in "blockage" as long as the difference between the input signal (the AO2 output) and the analogical signal, remade by the D/A C, is higher than 1 LSB of the first conversion.

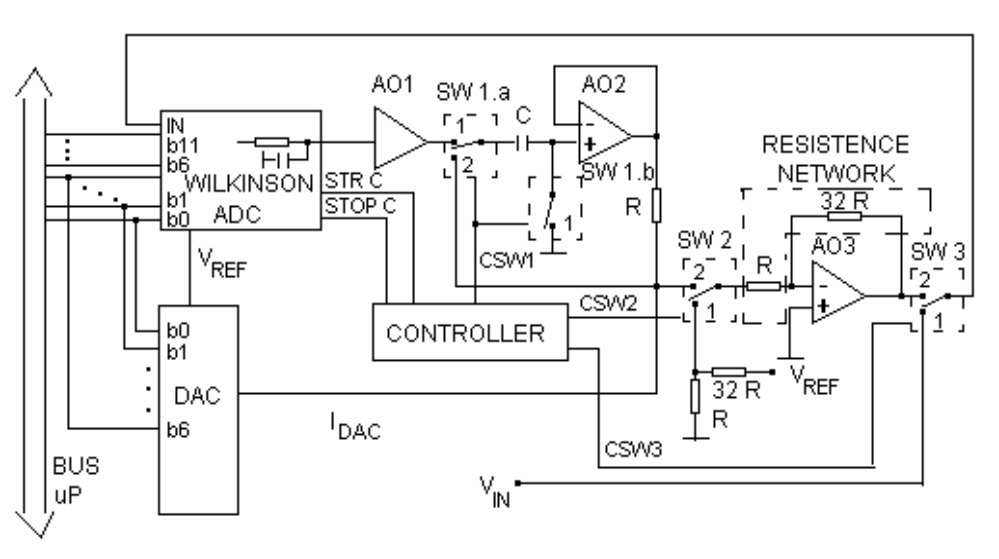

Fig. 5

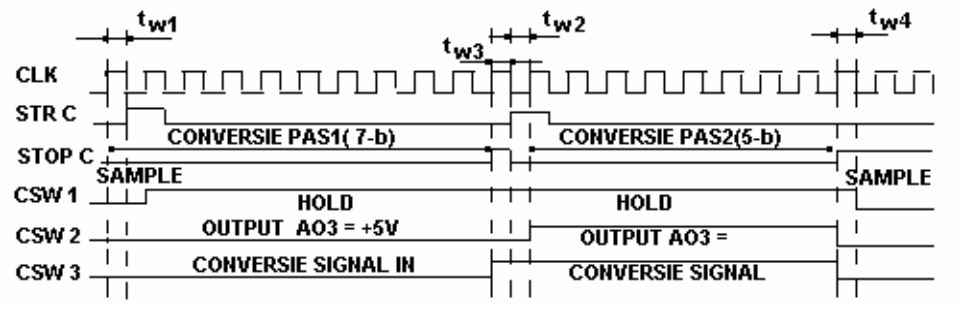

Fig. 6

5. IMPROVED PERFORMANCES OF W-RS CONVERTERS

The improved performance of the Wilkinson-Recursive Sub Ranging conversion method is presented in Fig. 7. Leaving the Wilkinson converter, the results of conversion from the first step (conversion by Wilkinson method) are stored in a buffer register CCR (coarse conversion register) respectively for the second step of conversion in FCR (fine conversion register), with the overlap of a bit a_7 from each register for performing digital correction (DC).

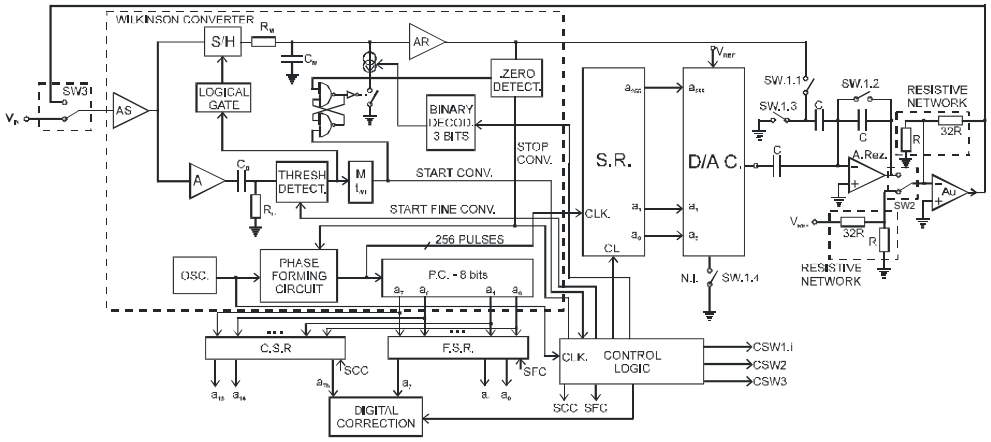

Fig. 7

The input signal held on the C_M capacitor during the period between the hold command and the current generator switching command, period which is controlled by the M monostabile, is held as well by the capacitor C_R of the A_{rez} residual amplifier input. After charging the C_R with the value of the input signal,

the switch S1.1 opens. During coarse conversion, the shift register SR changes its outputs to level 1 corresponding to the number of pulses generated by the clock. The digital code obtained in this way at the output of the shift register allows an easy digital to analog decoding by means of a set of switching capacitors [1–3].

After approximately 500 ns, time needed to perform the Wilkinson conversion on the first 8 bits, the switch S1.2. opens allowing to obtain at the output of the amplifier A_{rez} a residual voltage equal to the difference between the input signal V_{in} held on capacitor C_R and the analog value of input signal with a 8 bit resolution recovered through the measurement circuit-Wilkinson converter, shift register, D/A converter. In order to reduce leakage currents on holding capacitor C, a repeating amplifier RA with high output impedance is used. Pulses generated by the clock generator are converted in a counter PC.

Sequential control of W-RS must ensure control signals specific to the Wilkinson conversion as well as supplementary signals for performing the recursive conversion algorithm.

The signal diagram of the W-RS converter is presented in Fig. 8. The clock CLK_1 is a multiple of clock's pulse CLK ensuring the synchronization of starting and ending of charging for the holding capacitor C_M with respect to the oscillator's frequency. When threshold detection of the input signal occurs, with a delay given by the monostabile M_1 the input signal is held on the capacitor C_M and also on the capacitor C of the amplifier A_{rez} through the repeating amplifier AR (switches CSW1.2 and CSW1.3 are closed).

Having closed the switch SW1.4 one can hold the offset voltage of the amplifier A_{rez}, if previously a self-calibration has taken place [7]. The switch CSW2, non-active, ensures the output of amplifier A_u is at half of its output range and thus a shorter response time.

After generating the command START CONV. the Wilkinson conversion on the first 8 bits with digital storage of the input signal in a shift register SR is performed.

At the end of the coarse conversion the switch SW1.4 which allows the recovery of analog input voltage on 8 bits opens. Since the generation of this voltage in point D_0 also requires a settling time in order not to saturate or cut-off the output of amplifier A_{REZ}, the command of the switches SW1.2-SW1.3 has a t_{W2} delay.

The following notations were used:

t_{W1} – necessary time to settle output signal S/H, AR and charging signals A_{rez};

t_{W2} – necessary time to settle signal at the output of D/A converter in order not to saturate or cut the output of A_{rez};

t_{W3} – necessary time for a new start command of Wilkinson converter without detecting a new input pulse (internally generated);

t_{W4} – dead time for a new conversion, with offset cancellation for A_u and A_{rez};

– CCS, FCS – strobing coarse and fine conversion values in buffer register CCR and FCR;

– FCST – start generated by control logic for a new conversion (fine conversion) with no pulse at the input.

– CL – clear of shift register SR at the end of conversion.

After charging the coarse conversion register CCR with the digital value of the conversion in the first step by generating the command CCS (coarse conversion strobe) and activating the switch SW2, in order to amplify the residual voltage with a delay t_{W1} it is necessary to provide a new start command FCST of the Wilkinson converter without detecting the input pulse.

After performing the fine conversion in the second step, respectively conversion of residual voltage, the digital value is stored in FCR by the command of fine conversion strobing. During dead time t_{W4}, until a new start command is given, a cancellation of the offset voltage of the residual amplifier A_{rez} and the voltage amplifier A_u is performed with closed switches SW1.4 and SW1.3 and the CL command to bring to level zero the outputs of the shift register SR.

CLK_1 was chosen to be 10ns in order to ensure a sufficient time for settling the outputs of the residual and voltage amplifier, as well as for eliminating effects of transition processes. Synchronizing of start and end charging of the holding capacitor C_M is performed at clock's frequency CLK of 500 MHz. This cancels errors of differential non-linearity by reducing the even/odd effect.

By voltage amplification of the amplifier one can reduce residual voltage in the conversion range of the Wilkinson converter. By choosing the amplification $A_{rez} = 1$, a gain of 32 of the voltage amplifier A_u is needed in order to restore residual voltage to 1/8 of the range of the Wilkinson converter. Consequently control logic switches the constant current source digitally using a binary decoder (BD) to a current eight times less. Using a voltage amplifier A_n with small settling time and high slew rate, one can reduce the time of waiting to less than 10ns when passing from coarse to fine conversion by reducing the voltage range at the output of A_u.

Choosing the range of the Wilkinson converter 0÷10V, after the first step of the conversion on 8 bits the residual voltage is placed in the range 0÷39.06 mV (10V divided in 256 levels). By voltage amplification of 32 times the process reenters the second step in a reduced conversion range of Wilkinson converter (0÷1.25V). Wilkinson conversion in the second step determines the width of a conversion channel to reduce down to 4.88 mV.

Applying the principles of the recursive conversion method there is performed a second conversion named fine conversion for determining the remaining bits. Choosing the resolution of the conversion on both steps of 8 bits, and taking into account the overlapping of one bit in each step of the conversion for digital correction, a number of 32,000 channels is obtained. With a clock generator of 500 MHz the maximum conversion time during the two steps of

conversion – without taking into account other delays-becomes: $t_c = 2 \times 2^8 \times 2$ ns = = 1.028 μs.

This result corresponds to an average conversion time of 2MSPS. The new architecture exhibits some particularities of the conversion model:

– in order to cancel the offset voltage generated by comparators of D/A flash converter and taking into account Wilkinson conversion characteristics, one can replace the set of comparators by a shift register which controls a switching capacitors area for recovery of input voltage after the first step of conversion; that also allows usage of specific advantages of switching capacitors areas: simplicity, high slew rate, small size areas.

– by means of a specific sequential logic, we can ensure the usage of a residual amplifier with switching capacitors for subtracting as well as for holding the input voltage during the first step of Wilkinson conversion.

– in order to reduce the delay time between the first and second step of conversion, one can ensure a gain of 32 times of residual voltage within 39 mV– –12.5 V voltage range; at the same time, the leakage current is reduced eight times to maintain the same transfer function during both steps of conversion. Thus, a 4.88 mV channel width in the second step of conversion is obtained.

6. PERFORMANCE LIMITATIONS

The improvement of throughput rate performances is obvious with this method. Theoretically, we obtain the reducing of the effective conversion time from $2^{(p+q)}$ units specifically for Wilkinson conversion for a n bits conversion in two steps p and q ($n = p + q$) to ($2^p + 2^q$). This means for a Wilkinson ADC with a 100 MHz clock frequency reducing the conversion time from 40 μs to 1.56 μs, by a conversion of 7 + 5 bits in two steps.

Because of the dead times that appear in both methods, the effective conversion time increases, although not significantly. The timing diagram presented in Fig. 8, it result the increasing of the conversion time with tw1-tw4 that can be reduced to a maximal delay of 350 ns. Thus, the conversion time by this method has been found at about 1.9 μs.

In order to make this method applicable to spectrometric measurements, a substantial improvement of the differential linearity is necessary. There are several methods of reducing the INL error, which ensure the cancellation of the gain, offset and trimming mismatches. The most interesting part in this paper is the reduction of the DNL error. By using the digital correction, the DNL error typical for the recursive ADC's is 1/2 LSB, a value that is much too much for the proposed appliances. The main factors that influence the DNL error are given by the Wilkinson ADC-DAC group, that generates the first 7-b but also assures the reference scale for making the conversion in the next step (Fig. 2).

Choosing a 12-b Wilkinson converter with the DNL error less than 1% LSB for keeping the same mismatching error is necessary the 7-b D/A converter but 18-b precision at 100 ns settling time. Using AM 84 as 12-b Wilkinson ADC we obtain with the 100MHz clock frequency the INL error less 0.02%, the DNL error less 0.8% LSB and the time conversion 40 us on 12-b, 1.24 us on 7-b respectively 0.32us on 5-b. There also have been chosen high performance operational amplifiers with 300 V/μs slew rate and 0.01 % at 100 ns settling time.

The error due to gain of the AO3 op-amp can be canceled by self-calibration. Thus, for an op-amp with 50 mV/V open-loop gain, respectively A_u = = 50×10^3 at 32 closed-loop gain result $A_u < 0.064\%$ and it manifest as INL error.

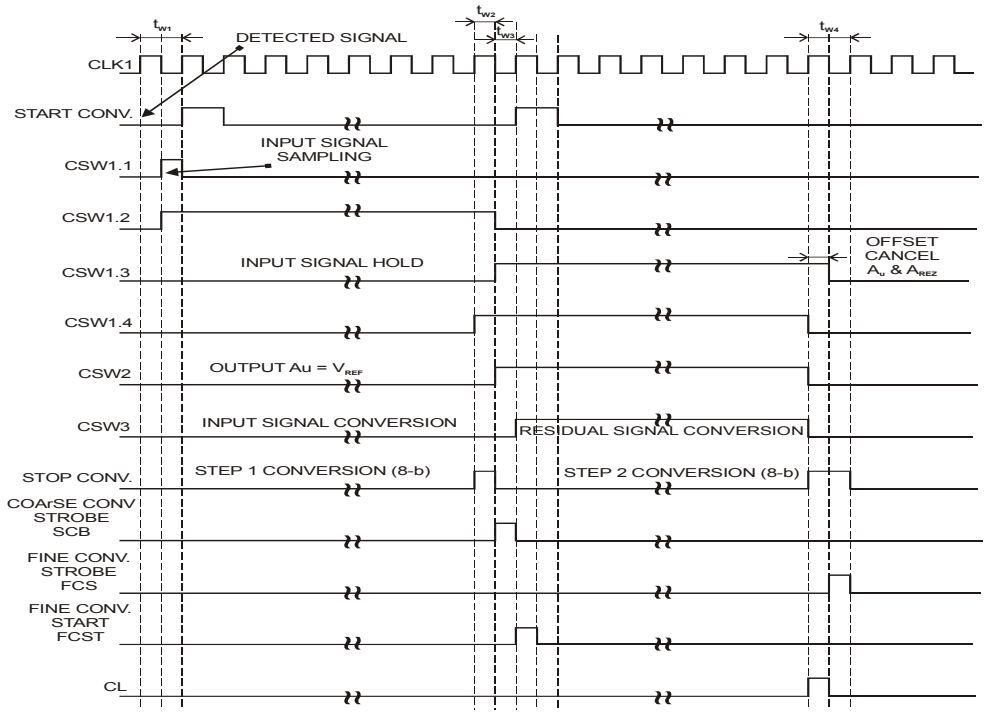

Fig. 8

In order to reduce the influence of the temperature we have used an R-2R resistive network in the AO3 loop-back with a variation temperature coefficient of less than 5 ppm/C.

The capacity used for the hold of input signal was made of a polycarbonate and polypropylene combination (200 pF) that has low dielectric absorption as well as a low temperature coefficient.

Choosing a switch with $R_{on} < 30$ Ohm, the follow error introduced by the capacity $C = 200$ pF with delay time $t_{w1} = 0.1$ μs is unimportant. As well, the droop rate in the hold period is less than 0.2% LSB, when choosing SW1 switch with a leakage current less than 100 pA and the AO2 op-amp with bias current less 120 pA.

Finally, the results point out that the main factors that influence the DNL error are the differential non-linearity errors introduced by the Wilkinson ADC and the D/A converter while simultaneously reducing the INL error by using various techniques of self-calibration.

7. CONCLUSIONS

With the new Wilkinson recursive ADC we indeed obtained a reduction of the effective conversion time, from $2(p + q)$ units down to $(2p + 2q)$ units, *i.e.* for an industry standard Wilkinson ADC with 100 MHz clock frequency the conversion time has been reduced from 40 μs to 1.9 μs. In comparison with the theoretical minimum value one can expect with this method, namely 1.56 μs, the difference corresponds to $t_{w1} - t_{w2}$ imposed delays.

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